UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,048	04/08/2004	Sadanand V. Deshpande	FIS920030397US1	3047

29154 7590 10/28/2005

FREDERICK W. GIBB, III
GIBB INTELLECTUAL PROPERTY LAW FIRM, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,048	DESHPANDE ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *15-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/08/04 9/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, (Claims 1-14) in the reply filed on October 6th, 2005 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **3 and 9** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, from which claim 3 depends, states, "first spacers adjacent said second gate conductors, and second spacers adjacent said first spacers". Claim 3 states the limitation "an etch stop layer positioned between said first spacers and said second spacers". Claim 8, from which claim 9 depends, states that the second-type transistors comprise "an etch stop layer on said first spacers, and second spacers on said etch stop layer". Claim 9 states the limitation that the "second spacers are only adjacent said first spacers" of the second transistor. In both claims 3 and 9, the two spacers cannot be adjacent if an etch-stop layer is between them.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims **1, 2, and 4-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Kao.

Regarding claim **1**, Kao discloses in Figure 5 an integrated circuit structure comprising: a substrate (100); first-type transistors (112) on said substrate, wherein said first-type transistors comprise first gate conductors (106b) and first spacers (114b) adjacent said first gate conductors; and second-type transistors (110) on said substrate, wherein said second-type transistors comprise second gate conductors (106a), said first spacers (114a) adjacent said second gate conductors, and second spacers (116b) adjacent said first spacers.

With regards to claim **2**, Kao discloses in Figure 5 the integrated circuit structure in claim 1, wherein said second spacers (116b) are only adjacent said first spacers (114a) that are adjacent said second gate conductors (106a), and said second spacers are not adjacent said first spacers (114b) that are adjacent said first gate conductors.

Regarding claim **4**, Kao discloses in Figure 5 and in column 3, lines 4-8 the integrated circuit structure in claim 1, further comprising: first-type impurity implants (108b) in areas of said substrate adjacent said first spacers (114b) of said first gate

conductors (106b); and second-type impurity implants (108a) in areas of said substrate adjacent said second spacers (116b) of said second gate conductors (106a).

With regards to claim **5**, Kao discloses in Figure 5 the integrated circuit structure in claim 4, wherein said first-type impurity (108b) is spaced closer to said first gate conductors (106b) than said second-type impurity (108a) is spaced from said second gate conductors (106a). Kao discloses in column 3, lines 4-8 that implants are placed in the substrate exposed by the spacer layers. Since transistor 112 in Figure 5 has one spacer layer (114b), and transistor 110 has two spacer layers (114a and 116b), one of which (114a) is the same thickness as 114b, it is inherent that the double spacer of transistor 110 is thicker. Therefore, the implants of transistor 110 are spaced farther from the gate than those of transistor 112.

Regarding claim **6**, Kao discloses in column 3, lines 4-8 the integrated circuit structure in claim 4, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

Regarding claim **7**, Kao discloses (column 2, lines 25-29) the integrated circuit structure in claim 1, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims **3, and 8-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Krivokapic. Claims 3 and 9 are rejected as best understood in light of the 112(2nd) rejection previously discussed.

Regarding claims **3, 8, and 10**, Kao discloses in Figure 5 an integrated circuit structure comprising: a substrate (100); first-type transistors (112) on said substrate, wherein said first-type transistors comprise first gate conductors (106b) and first spacers (114b) adjacent said first gate conductors; and second-type transistors (110) on said substrate, wherein said second-type transistors comprise second gate conductors (106a), said first spacers (114a) adjacent said second gate conductors.

With regards to claim **3**, Kao does not disclose an etch stop layer positioned between said first spacers and said second spacers, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors.

With regards to claim **8**, Kao does not disclose an etch stop layer on said first spacers of the second transistor, and that second spacers (116b) are on an etch stop layer.

Regarding claim **9**, Kao does not disclose wherein said second spacers are only adjacent said first spacers that are adjacent said second gate conductors and not adjacent said first spacers that are adjacent said first gate conductor.

Regarding claim **10**, Kao does not disclose wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors.

Krivokapic teaches in Figure 2D a double spacer (items 20 and 33) on a p-channel device, separated by an oxide liner (38) that is used as an etch stop during the etch-back of spacer 33 (col 5, ln 19-23). The etch stop is not present on the n-channel device. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the structures taught by Kao and Krivokapic, due to the fact that an etch stop layer allows separate materials to be chosen for spacer layers in order to optimize drive current in each type of device (Krivokapic col 6 ln 1-5). The resulting structure from such a combination is a CMOS device, where the p-channel transistor contains two spacer layers to widen the channel, with an etch-stop layer between the spacers. This resulting structure satisfies the claim limitations of claims 3, 8, 9, and 10.

Regarding claim **11**, Kao in view of Krivokapic discloses the integrated circuit structure in claim 8 further comprising: first-type impurity implants (Kao Figure 5, item 108b) in areas of said substrate adjacent said first spacers of said first gate conductors

(112); and second-type impurity implants (Kao Figure 5, item 108a) in areas of said substrate adjacent said second spacers of said second gate conductors (110).

With regards to claim **12**, Kao in view of Krivokapic discloses (Kao Figure 5) the integrated circuit structure in claim 11, wherein said first-type impurity (108b) is spaced closer to said first gate conductors (106b) than said second-type impurity (108a) is spaced from said second gate conductors (106a). Kao discloses in column 3, lines 4-8 that implants are placed in the substrate exposed by the spacer layers. Since transistor 112 in Figure 5 has one spacer layer (114b), and transistor 110 has two spacer layers (114a and 116b), one of which (114a) is the same thickness as 114b, it is inherent that the double spacer of transistor 110 is thicker. Therefore, the implants of transistor 110 are spaced farther from the gate than those of transistor 112.

Regarding claim **13**, Kao in view of Krivokapic discloses (Kao column 3, lines 4-8) the integrated circuit structure in claim 11, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

With regards to claim **14**, Kao in view of Krivokapic discloses (Kao column 2, lines 25-29) the integrated circuit structure in claim 8, wherein said first-type transistors comprise n-type field effect transistor and said second-type transistors comprise p-type field effect transistors.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hung discloses a method for manufacturing CMOS devices with

offset spacer structures. Cheek discloses using spacers to self-align source and drain regions around transistors. Ju also discloses a method of forming transistors with spacers being used to define channel length. Finally, Komori discloses a method for forming transistors with different breakdown voltages and fixed offsets.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jci

GEORGE ECKERT
PRIMARY EXAMINER